3320
64 BIT-4Ø-SHIFT REGISTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3320 is a 64 bit dynamic shift register plus logic for loading or recirculating information within the circuit. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement mode MOS technology.

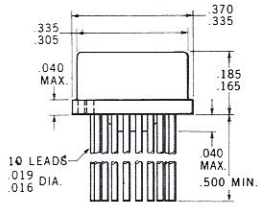
ABSOLUTE MAXIMUM RATINGS

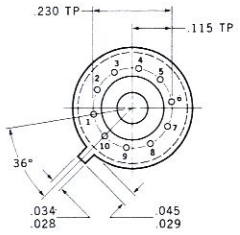
- **CLOCK VOLTAGES (ϕ_1, ϕ_2, ϕ_3, ϕ_4) . . . —30 V to +0.3 V**
- **DATA INPUT AND STORE VOLTAGES . . . —30 V to +0.3 V**
- **STORAGE TEMPERATURE . . . . . —55°C to +150°C**
- **OPERATING TEMPERATURE RANGE . . . —55°C to +85°C**

FEATURES

- **LOW POWER — 200 μW/BIT AT 2.0 MHz**
- **INPUT STORE AND ENTER CONTROL LOGIC**
- **DATA AND DATA COMPLEMENT OUTPUT**
- **INPUT GATE PROTECTION**
- **TYPICALLY 3.0 VOLT NOISE MARGIN**

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)

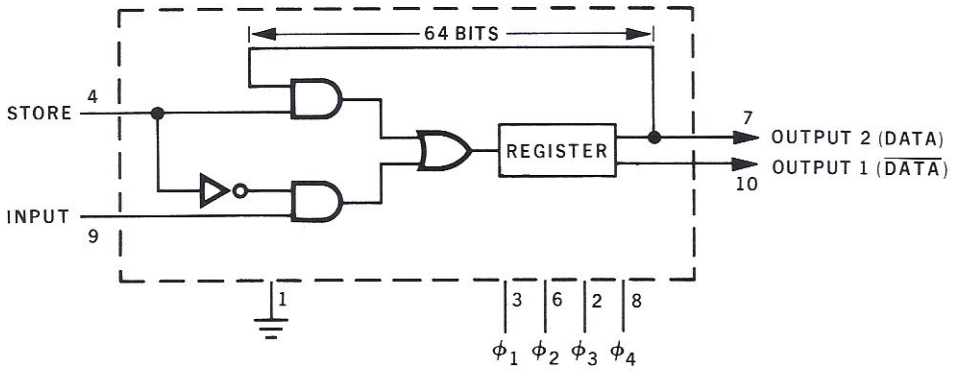


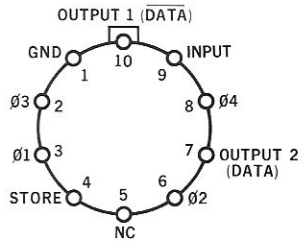


NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F332014X

CONNECTION DIAGRAM





TOP VIEW

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS Standard Conditions (unless otherwise specified)
Load = 10 MΩ and 10 pF, $T_A = -55°C$ to $+85°C$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Clock Repetition Rate	0.01		2.0	MHz	
	Clock Pulse Width (ϕ_1 & ϕ_3)	100			ns	at −24 Volts } See
	Clock Pulse Width (ϕ_2 & ϕ_4)	200			ns	at −24 Volts } Figure 1
V_{CP}	Clock Logic Levels					
	Logic "0"	+0.3		−1.0	Volts	
	Logic "1"	−24		−27	Volts	
V_{IN}	Data and Store Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−10		−24	Volts	
	Data Input Pulse Width	100			ns	Stable During t_{mp} See Figure 1
	Store Pulse Width	200			ns	Stable During t_{sr} See Figure 1
C_C	Clock Input Capacitance					
	ϕ_1, ϕ_3		15		pF	
	ϕ_2, ϕ_4		10		pF	Plus Output Capacitive Load
C_{IN}	Data and Store Input Capacitance		2.0		pF	
I_{LCP}	Input Leakage to Ground					
	ϕ_1, ϕ_2, ϕ_3, ϕ_4			100	μA	$V_C = -27$ V
I_{LX}	Data and Store Terminals			1.0	μA	$V_{IN} = -20$ V
	Output Logic Levels					
V_{OL}	Logic "0"	0		−2.0	Volts	
V_{OH}	*Logic "1"	−11		−24	Volts	
	Power Per Bit**		0.2		mW	at 2.0 MHz
	Power Per Output Buffer		10		mW	at 2.0 MHz and 10 pF Load

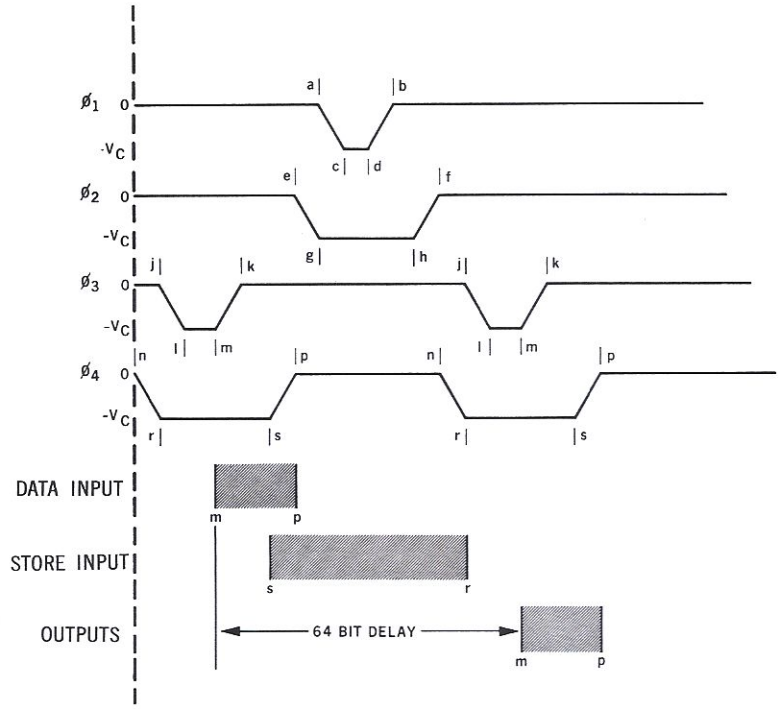
*NOTE: A resistive load to ground will have the effect of discharging the output level (Logic "1") to ground with a time constant equivalent to the RC time constant of the external load.

**NOTE: The power dissipation of each of these stages decreases proportionally with frequency.

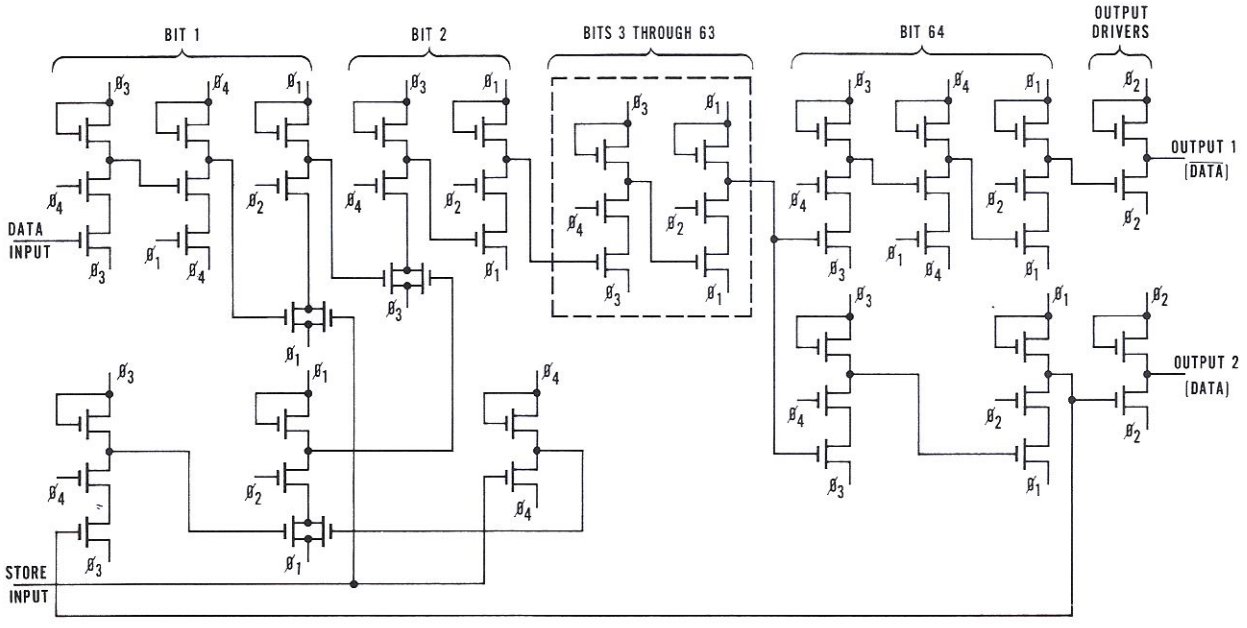
MINIMUM CLOCK REQUIREMENTS

CHARACTERISTIC	SYMBOL	MIN. VALUE (ns)	MAX. VALUE (μs)
ϕ_1 Pulse Width	t_{cd}	100	
ϕ_3 Pulse Width	t_{lm}	100	
ϕ_2 Pulse Width	t_{gh}	200	
ϕ_4 Pulse Width	t_{rs}	200	1.0
Sampling Width 1	t_{bh}	100	
Sampling Width 2	t_{ks}	100	
ϕ_4 - ϕ_1 Overlap	t_{pa}	0	
ϕ_2 - ϕ_3 Overlap	t_{fj}	0	
ϕ_2 - ϕ_4 Overlap	t_{fn}	0	1.0
ϕ_4 - ϕ_2 Overlap	t_{pe}	0	
ϕ_3 Precharge Time	t_{rm}	100	
ϕ_1 Precharge Time	t_{gd}	100	

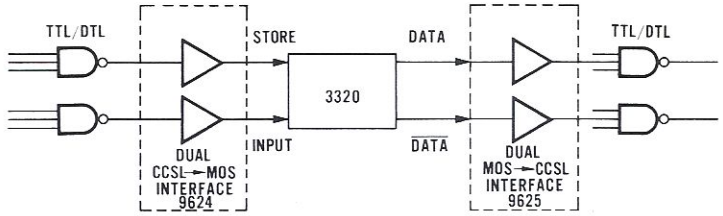
FIG. 1 — TYPICAL WAVEFORMS

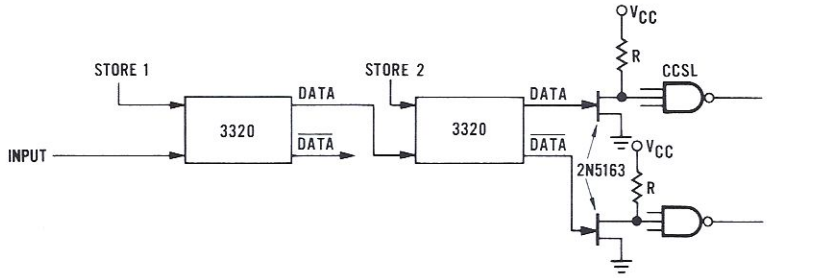


SCHEMATIC DIAGRAM



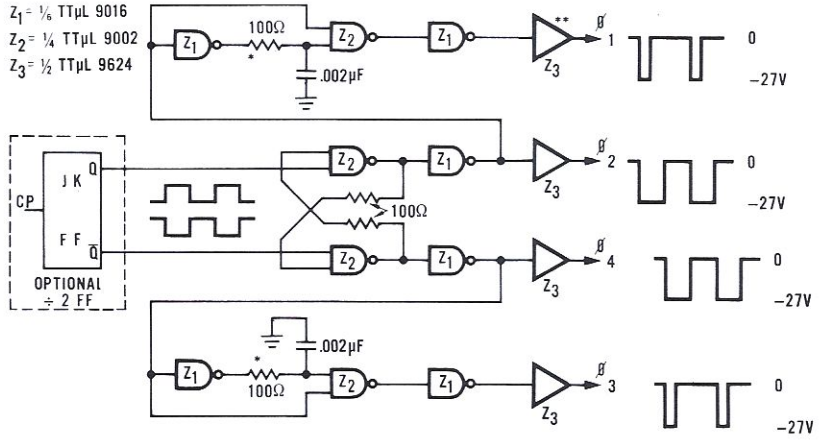
TYPICAL INTERFACE AND INTERCONNECTION DIAGRAM



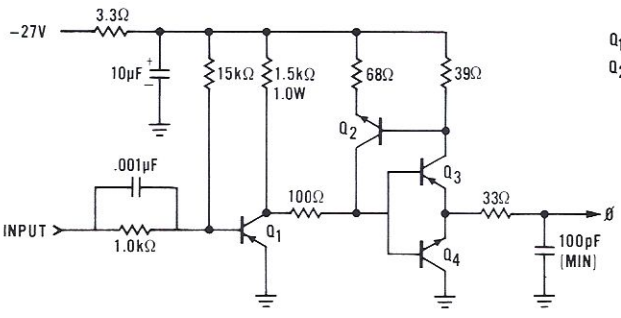


EXTERNAL R≥ 10kΩ
FOR IMPROVED NOISE MARGIN
TO CCSL.

4ø CLOCK GENERATOR



* PRECHARGE ONE SHOTS WITH R = 100 Ω & C = .002 μF FOR ~ 80 ns PRECHARGE PULSE.



Q1,Q3 = 2N3644
Q2,Q4 = 2N3641

**OPTIONAL BIPOLAR TO MOS INTERFACE WHERE HEAVY DRIVE CAPABILITY IS REQUIRED.

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